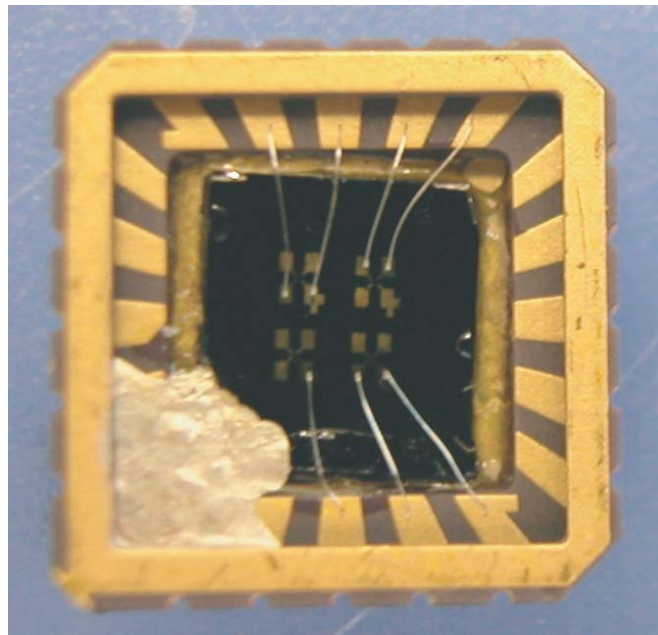

Electrical Transport through Single Walled Carbon Nanotubes Grown by the Chemical Vapour Deposition Method

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Chapter 1

Introduction

1.1 The Discovery of Carbon Nanotubes

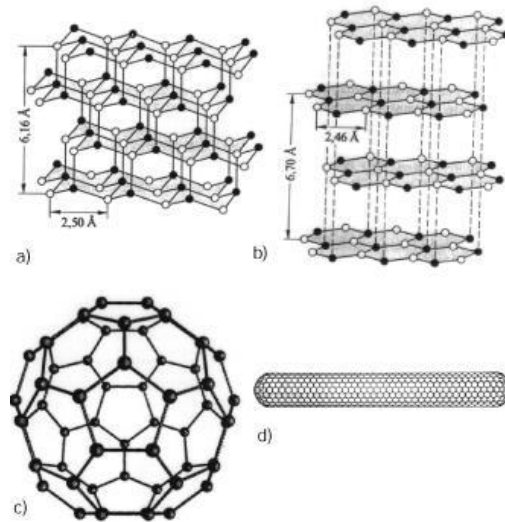
In August 1985, Harry Kroto of the University of Sussex and Richard Smalley from Rice University were the first to observe the formation of the C_{60} molecule [1]. This might have been the start to a new and promising branch of physics, but it was hardly a surprise to scientists all over the world. Long before that, chemists and physicists had been wondering why the versatile carbon atom could only be found in two kinds of structures - graphite and diamond. There had been propositions by Roald Hoffmann, Orville Chapman e.a. as to what forms ought to be observable, but every attempt to create these structures had failed.

So it was Kroto and Smalley who incidentally made the discovery while working on laser evaporation. They met with some of their students at Rice in 1985 to find out what would happen during carbon evaporation. The result seemed odd: By far the greatest part of the carbon settled as C_{60} which did not make a lot of sense at first. Then it was recognized that out of sixty carbon atoms a very stable, football-shaped molecule could be formed. The idea proved to be correct. A new form of carbon crystal had been discovered. The first publication was printed in November 1985 in "Nature".

In order to investigate this new state of carbon though, a method had to be found first to produce it in sufficient quantity. Wolfgang Krätschmer and Donald Huffman were successful in this with a carbon arc instead of a laser. The soot that settled at the base of the apparatus during evaporation was dissolved in benzene and dried. The product consisted of C_{60} (90%) and C_{70} (10%). With this a vital condition for further proceeding was fulfilled.

In 1991 finally, Sumio Iijima from NEC-labs in Japan 'discovered' nanotubes [2]. These devices had been observed before, but Iijima was the first to understand their true nature: Tiny cylinders out of carbon with caps at both ends. The caps turned out to be in most cases a C_{60} molecule split in two halves either perpendicular to one of the hexagonal or one of the pen-

Figure 1.1: Different kinds of carbon structures. a) Diamond is a very stable carbon lattice. b) Graphite consists of layers of graphene sheets. The distance between two layers is significantly greater than the distance between two neighboring atoms in the plane. c) C_{60} molecules form when evaporated carbon settles on surfaces. d) Nanotubes can be figured as a graphene sheet rolled into a cylinder and closed at each end by half a C_{60} molecule. Taken from [3]



tagonal sides. Every row of the cylinder then contains 9 or 10 carbon atoms respectively, so that as an example a C_{70} molecule is formed by inserting into a C_{60} molecule one row of atoms perpendicular to one of its pentagonal sides. The two cases are designated as "zigzag structure" and "armchair structure", referring to the form of each row.

1.2 Why are we interested in Carbon Nanotubes?

It soon became clear that carbon nanotubes (CNT) are unique in several ways that make them ideal candidates for a number of applications in industry and research. Their very high flexibility and strength for instance could prove valuable for usage as sensors in scanning force microscopes, but makes them also a perfect basic material wherever something needs to be strong and light at the same time.

Beyond their mechanical characteristics, nanotubes show some amazing electrical behaviour. As explained in the following theoretical part of this text, nanotubes can be either metallic conductors or semiconductors de-

pending on their chirality [4]. Metallic nanotubes are considered the smallest known conducting wires [5], while semiconducting nanotubes can act as field effect transistors. Unfortunately though, there is no reliable way of growing nanotubes selectively. Such a method would simplify many processes by allowing to grow just the type of nanotubes one needs for a certain application.

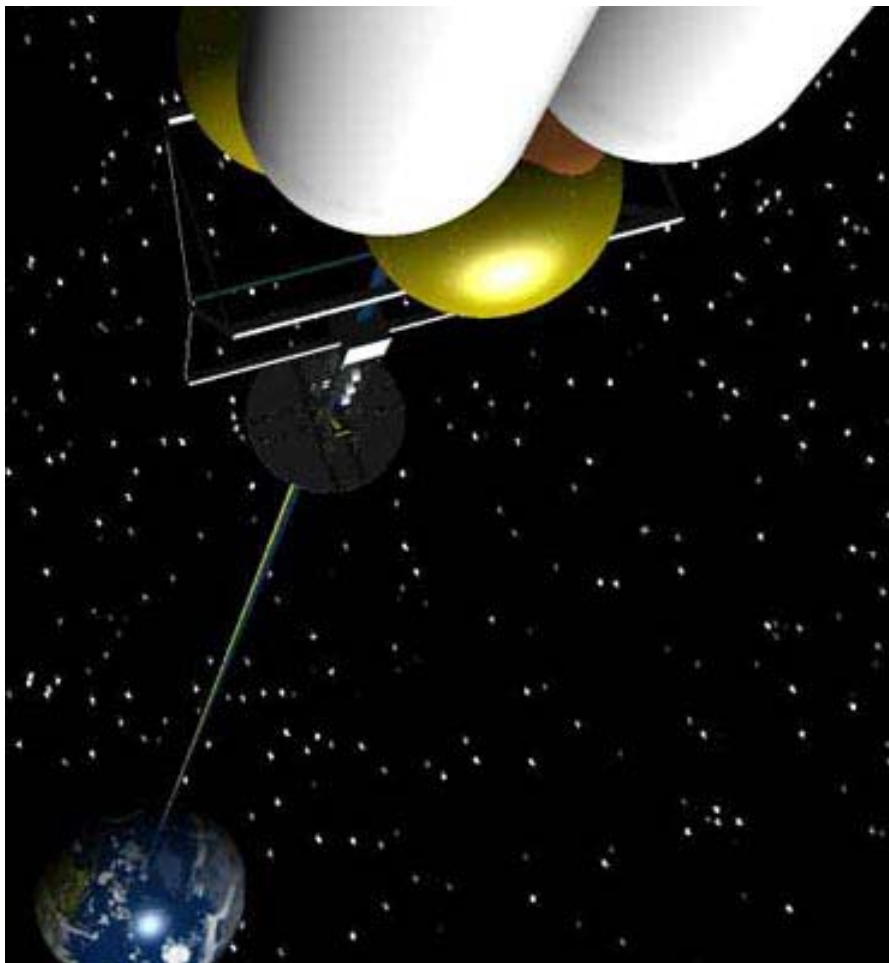


Figure 1.2: One of the more fantastic applications of carbon nanotubes proposes an elevator into orbit. Nanotubes would be light and strong enough to provide the material for the cable. Taken from [6].

Chapter 2

Theory

2.1 The Tight Binding Approximation for SWNT

A thorough understanding of the behaviour displayed by single-wall nanotubes (SWNT) requires first of all an analysis of their atomic structure, which is closely related to other carbon structures [4]. Nanotubes can be thought of as sheets of graphite rolled into a cylinder and closed at both ends by caps (see Fig. 2.1). Graphite consists of carbon atoms arranged in a hexagonal lattice plane with a lattice constant of $a = 1.42$ nm. Of the four valence electrons of graphite, only one contributes to conductance. It is in the $2p_z$ state, its axis of symmetry perpendicular to the lattice plane.

We will now look at the problem from the viewpoint of the "tight binding approximation". As the unit cell of a hexagonal lattice contains two atoms we designate by A and B , we can write the total wave function as

$$\psi = \varphi_1 + \lambda\varphi_2 \quad (2.1)$$

where

$$\varphi_1 = \sum_A \exp [2\pi i \vec{k} \cdot \vec{r}_A] X(r - r_A)$$

is the sum of the normalized orbital $2p_z$ wave functions $X(r)$ over all A -atoms and analogical

$$\varphi_2 = \sum_B \exp [2\pi i \vec{k} \cdot \vec{r}_B] X(r - r_B)$$

the sum over all B -atoms. By assuming the overlap of the atomic wave functions $\int X(r - r_A) X(r - r_B) d\tau$ to be small, we can proceed by substituting (1) into $H\psi = E\psi$ and multiplying this equation once by φ_1 and once by φ_2 . By integrating both products and eliminating λ we can solve the resulting equation system for E as:

$$E = \frac{1}{2S} \{ H_{11} + H_{22} \pm ((H_{11} - H_{22})^2 + 4|H_{12}|^2)^{\frac{1}{2}} \} \quad (2.2)$$

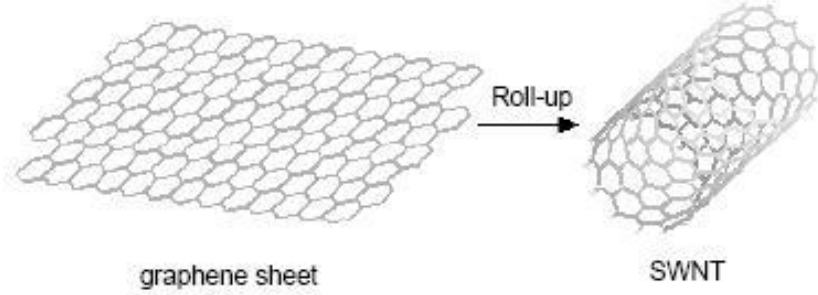


Figure 2.1: By rolling a graphene plane into a cylinder, we get a single-wall nanotube (SWNT). This model allows for quantitative calculations of the band gap. Taken from [5]

where

$$H_{ij} = \int \varphi_i^* H \varphi_j d\tau$$

and

$$S = \int \varphi_1^* \varphi_1 d\tau.$$

For reasons of symmetry, $H_{11} = H_{22}$, and by defining

$$H'_{ij} = \frac{1}{N} H_{ij}$$

with $N = S$ the number of unit cells we finally write above equation as

$$E = H'_{11} \pm |H'_{12}|. \quad (2.3)$$

Since the negative sign refers to the inner rim of the first Brillouin zone and the positive sign to the outer rim, the discontinuity across the zone boundary is found to be

$$\Delta E = 2|H'_{12}|. \quad (2.4)$$

This energy discontinuity can be calculated inserting the relevant lattice vectors and assuming that every A -atom interacts only with its three neighboring B -atoms and vice versa. Defining further the nearest-neighbor overlap integral

$$\gamma_0 = \int X^*(\vec{r} - \vec{A}\vec{B})(U - V)X(\vec{r})d\tau > 0$$

and using V for the periodic potential of the lattice as well as U for the potential field for an isolated atom, we get

$$|H'_{12}|^2 = \gamma_0^2 \left(1 + 4 \cos^2\left(\frac{1}{2}k_x a\right) + 4 \cos\left(\frac{1}{2}k_x a\right) \cos\left(\frac{1}{2}k_y \sqrt{3}a\right) \right). \quad (2.5)$$

2.2 Chirality and Electrical Conductance

This analysis was done originally by P. R. Wallace in 1946 for graphite, long before the discovery of nanotubes. So why does it matter? As stated in the beginning, the cylinder wall of a nanotube is in principal a sheet of graphene rolled along a certain axis. The direction of that axis and the diameter of the resulting cylinder can be specified by the vector $\vec{c}_h = n_1\vec{a}_1 + n_2\vec{a}_2 \equiv (n_1, n_2)$, where $n_{1,2}$ are integers and $a_{1,2}$ the unit vectors of graphene. As shown in Fig. 2.2, \vec{c}_h connects two cristallographically equivalent sites A and A' of the plane. By connecting these two sites, the "chirality" of the nanotube is fixed and \vec{c}_h becomes a ring around the cylinder surface perpendicular to the axis direction. The diameter of the nanotube cylinder amounts to

$$d = |\vec{c}_h|/\pi = a\sqrt{n_1^2 + n_1n_2 + n_2^2}/\pi,$$

and the so-called chiral angle is given by

$$\theta = \arctan[-\sqrt{3} \cdot n_2/(2n_1 + n_2)].$$

Nanotubes do not always grow in the same way: Depending on the side around which the initial cap is growing (pentagonal or hexagonal) and on defects in the early growth, the tube may have any chiral angle between $\theta = 0^\circ$ [$(n_1, n_2) = (p, 0), p \in \mathbb{Z}$] and $\theta = \pm 30^\circ$ [$(n_1, n_2) = (2p, -p), (p, p)$] [7]. The first case is called the "zigzag direction", the second "armchair direction" because of the atom configuration. All other chiral angles yield the same result as an angle between -30° and 30° due to the rotational periodicity of the hexagonal lattice. We therefore choose $|\theta| \leq 30^\circ$ or analogically $-n_1 \leq n_2 \leq n_1$ for our definition.

Let us now return to our formula for the band gap at the boundary of the first Brillouin zone:

$$|H'_{12}|^2 = \gamma_0^2(1 + 4\cos^2(\frac{1}{2}k_x a) + 4\cos(\frac{1}{2}k_x a)\cos(\frac{1}{2}k_y\sqrt{3}a)).$$

A nanotube has a 1D periodic structure along its axis. In radial direction the wave function of the electrons is restricted by the one-atom thickness of the plane, in axial direction the 2D energy dispersion (5) is reduced by one degree of freedom by the periodic boundary condition

$$\vec{c}_h \cdot \vec{k} = 2\pi m, m \in \mathbb{Z} \tag{2.6}$$

so that we get 1D energy bands.

If we insert into equation (5) as k_x, k_y the coordinates of the edges of the first Brillouin zone we find that for these vectors the band gap amounts to

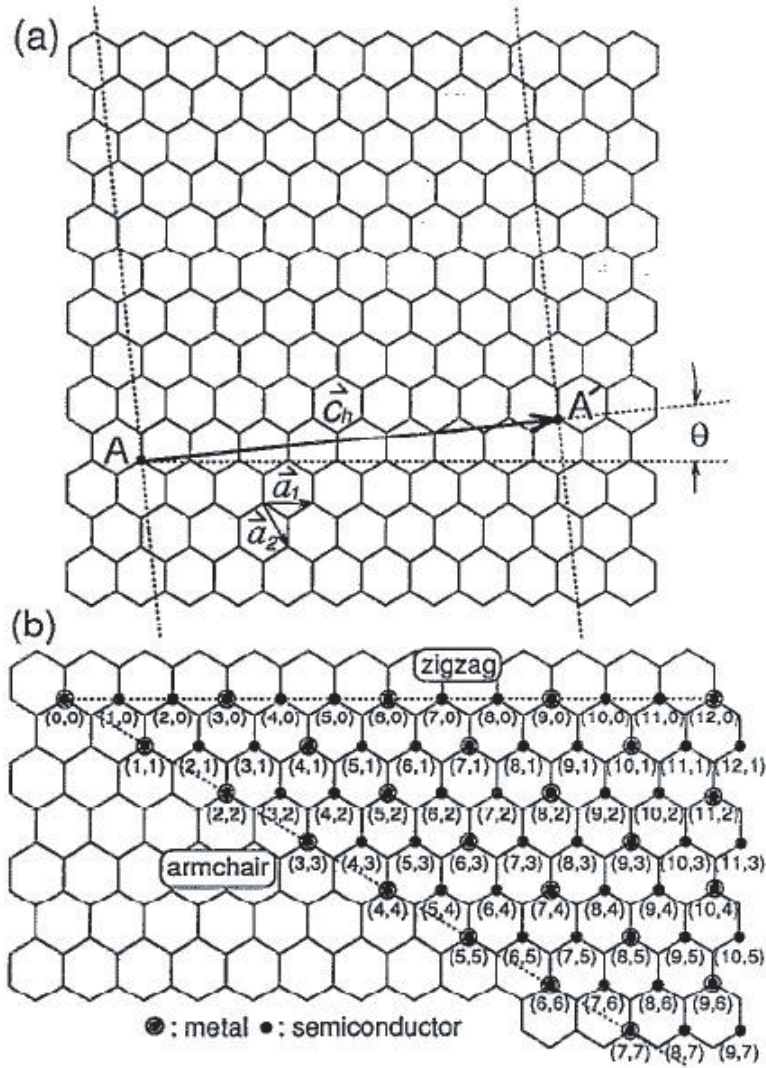


Figure 2.2: a) The two almost vertical lines are seams. By rolling the graphene plane in such a way that they are connected, we get a cylinder. The angle θ determines the direction of the rolling. We call θ the "chiral angle". b) As shown in the text, the chiral vector \vec{c}_h determines the electronic properties of the nanotube. In this figure \vec{c}_h is represented by the coordinates of its end point. Taken from [2]

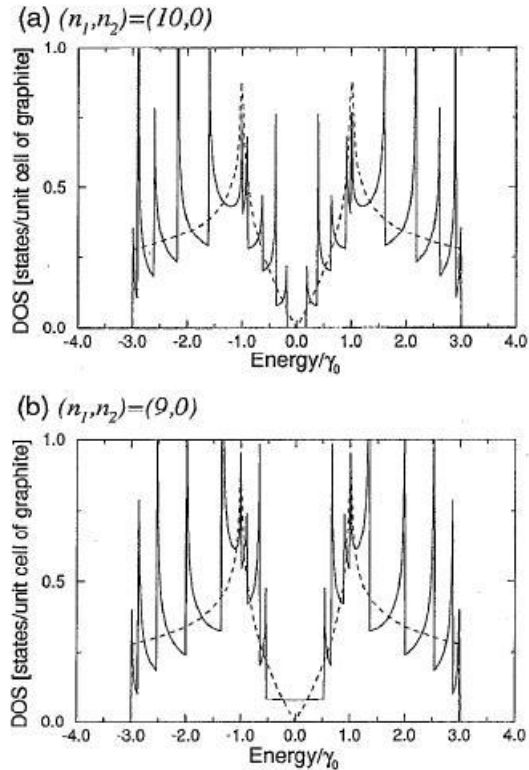


Figure 2.3: a) Electric density for a SCSWNT in our approximation. b) Density for a metallic tube. Taken from [7]

zero and we consequently get a metallically conducting nanotube. Combining this condition with equation (6) we obtain as a final result the formula

$$2n_1 + n_2 = 3q, q \in \mathbb{Z} \quad (2.7)$$

for metallic tubes. We expect all other nanotubes to be semiconducting as for them we calculate a non-vanishing band gap (Fig. 2.3).

2.3 Quantum Dots at Low Temperatures

Although it was not possible to detect Coulomb oscillations with my nanotube samples, it seems necessary to say something about them in order to explain the experimental setup.

A SWNT can act as a quantum dot. As described in the next chapter, our nanotubes are in electrical contact with a source line and a drain line. The coupling to the source and drain contacts is assumed to be small enough to

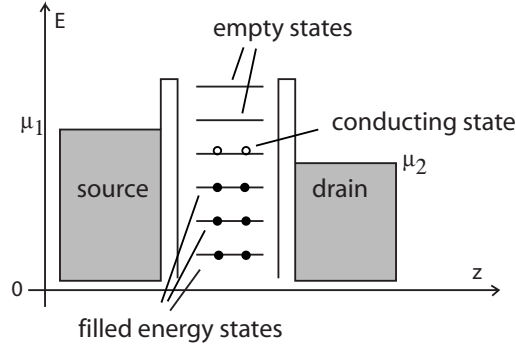


Figure 2.4: Schematic for conductance through the allowed energy states on a quantum dot.

turn the SWNT effectively into an island for electrons (for $G < e^2/h = G_Q$). At any given time, the number of electrons on the nanotube will be an integer number N . Electrons can enter or leave this island depending on the source/drain voltage and the capacitance of the tube. The capacitance is connected to the charging energy $E_C = e^2/(2 \cdot C_{tot})$, the energy which must be invested to add an electron to the quantum dot (i.e. the nanotube) [8].

The very close confinement of electrons on a nanotube turns the continuous energy spectrum into a set of discrete energy eigenstates. Because of this, conductance through a nanotube quantum dot can only occur through the allowed electron energy states of the device [9]. As depicted in Fig. 2.4, all states that are energetically lower than both the source and the drain contact are filled with two electrons each (spin degeneracy). The states that are too high will not participate because the occupation density is very low for them. Only states that are close enough to the electrochemical potential of the contacts can take part in conductance, because electrons can only flow when free states are available in the drain metal. At very low temperatures and for $\mu_1 > \mu_2$, conductance will therefore only occur when one allowed energy state of the nanotube is very close to μ_2 . The energy of these states can be manipulated with a backgate voltage that creates a uniform field around the nanotube and thus controls the chemical potential of the dot.

At any temperature $T > 0$ the Fermi function is smeared due to thermal energy. The range of this effect is about $3.5 \cdot k_B T$ while the level spacing for a nanotube is given by $\Delta E = \frac{h v_F}{2L}$ with $v_F = 8 \cdot 10^5 \frac{m}{s} = 2.65 \cdot 10^{-22} J$ for $L = 1 \mu m$. As soon as the temperature of the device is significantly smaller than 10 K, the thermal energy will not be sufficient to smear the states completely and gaps will become visible where the tunneling rates are low.

Chapter 3

Growing and Contacting Carbon Nanotubes

The technique for producing a good nanotube sample requires many steps that have to be carried out carefully and with outmost precision if the result is to be satisfying. Needless to say that I depended on help even at the end of this project. The parameters and settings of the numerous machines and programs were won over the years by experience - I simply used the parameters I was recommended. All relevant data are listed in the appendix.

3.1 Cutting and Cleaning the Si-Wafer

The nanotubes were grown on a highly doped Si-wafer with a 400 nm thick SiO_2 insulation on top of it (100 nm for the later sample). Squares with a side length of about 2 cm were gained by scratching the original plate with a diamond cutter and breaking it into convenient pieces. These pieces were subsequently cleaned by placing them first in a ultrasonic cleaner within some 2-propanol, then in a UVO-cleaner (Model 42 by Jelight Company, Inc.) and finally in an Oxygen Plasmalab^{80Plus} by Oxford . In this way it was hoped to remove all pieces of dirt from the wafer that would later cause problems.

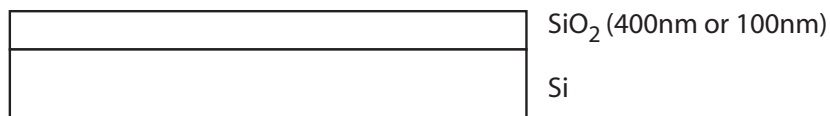


Figure 3.1: The wavers consist of Si with either 100 nm or 400 nm of isolating SiO_2

3.2 Growing the Nanotubes

In order to make carbon atoms stick to the SiO_2 -surface and grow into tubes, a catalyst was spun onto the wafer. This was done with a rotating plate (spinner) onto which the wafer had been fastened by means of a light vacuum from below. The catalyst fluid was shaken ultrasonically during two hours, then stood for ten minutes to let bigger particles sink to the ground. One or two drops of the catalyst were deposited on the surface after the plate was set into fast rotation by a predefined program. In this way the catalyst was dispersed as a thin film on the surface.

The chemical vapor deposition process (CVD) itself took place in a small oven into which the wafer was inserted on a long spoon. The oven was sealed and flooded with argon through a hose to prevent air (especially water) from entering the chamber during the process. The oven was heated up to 1000°C while argon was flowing through it, then the argon flow was replaced by hydrogen. With hydrogen still flooding the chamber, methane was added for exactly ten minutes to provide carbon atoms for the nanotubes which during this short period formed on the surface. After that time the methane was turned off and argon again turned on. The heating was switched off and the oven cooling down to 550°C , at which point the hydrogen was turned off and the oven cooling further with only argon flowing through. When the temperature had dropped below 300°C the oven was opened and the sample removed. The SiO_2 -wafer was now covered with nanotubes (Fig. 3.2), but they still had to be localized exactly and contacted with electron beam lithography.



Figure 3.2: At 1000° Celsius, carbon atoms from methane gas stick to the surface of the wafer, growing into nanotubes.

3.3 Localizing and Contacting the Nanotubes

The work during this project included the usage of two scanning electron microscopes. A LEO 15XX by Gemini was used for imaging only, while electron beam lithography was done with a JEOL JSM-IC848.

After CVD, the sample was inspected with the LEO microscope to tell whether the yield of nanotubes met the expectations. The exact position of the tubes was not determined in this step.

After successful growth had been verified, the sample was covered with a layer of PMMA (Polymethylmethacrylat). This was achieved in much the same way as the film of catalyst earlier, except that the PMMA was applied to the surface before spinning. Then the sample was baked in an oven under 180° C for at least 45 minutes in order to polymerize the PMMA (Fig. 3.4a)). After cooling down, the sample was inserted into JEOL. With the electron beam of the microscope, two structures were burned into the PMMA (Fig. 3.4b)): Four pads that were to serve later as contacts for the bonding wires, and between each quartet of pads a field of much smaller crosses that could be used as reference points when localizing single tubes. Both structures were created with the program PROXY WRITER on a computer and written automatically once the focus of the beam and all relevant parameters had been adjusted. The whole wafer contained 16 of those units, arranged in a four-by-four array. After removing the sample from JEOL, these structures were chemically developed in E-beam resist developer and isopropanol (Fig. 3.4c)).

The next step consisted in adding layers of the materials chosen for the pads. Since contact of the pads with random nanotubes had to be prevented (danger of shortcuts) a layer of isolating SiO₂ was applied first, then some Ti and on top of that 60 nm of Au as a conductor. The application was done with a Balzers-Pfeiffer PLS 500 evaporator. The materials were placed in pockets and heated by an electron beam. This caused a fine vapor in the previously evacuated chamber that settled on all surfaces. The sample had been built into the chamber opposite to the pocket and was therefore covered with a thin film of the evaporated material (Fig. 3.4d)). The rate and final thickness of the film was set with a Telemark deposition controller model 880. The sample was subsequently rinsed in acetone to dissolve the remaining PMMA. All the material on top of PMMA was removed along with it and only the areas freed of PMMA before the evaporation kept the film of SiO₂, Ti and Au (Fig. 3.4e)).

The sample was then investigated through the LEO electron scanning microscope once more. This time individual nanotubes were chosen as candidates for contacting. Only tubes roughly in the center of four pads were of interest and those with an appearance suggesting a single-wall nanotube (SWNT). The position of every candidate was marked with respect to the grid of crosses.

In order to provide connection between the pads and the nanotube in the center of them, another conducting structure had to be created (compare with Fig. 3.7). In the case of the first sample, this inner structure simply consisted of a source running from the two pads on the left to the tube, and a drain line connecting the opposite side of the tube to the remaining two

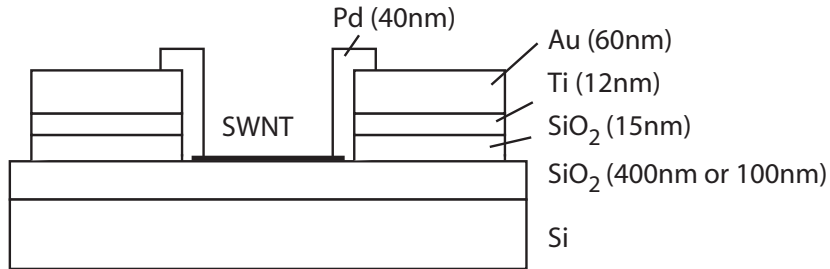


Figure 3.3: Using electron beam lithography, conducting structures are applied to the surface. They serve as contacts between the experimental setup and the SWNT.

pads on the right. For the second sample, the inner structure also included a middle contact and a topgate. The source and drain parts, however, did not yet touch the nanotube itself, since the insulating layer of SiO_2 would have prevented conduction anyway. To create these structures, the whole process with PMMA application, electron beam writing and evaporation was repeated. Finally, a layer of small palladium pads was added to provide conductance between the nanotube and the inner structure (Fig. 3.3). Palladium pads also made sure the original large pads were connected to the inner structure, since until then the SiO_2 layer of the inner structure had prevented conduction between the two gold layers. This was done in a third step, again complete with PMMA, writing and evaporation.

3.4 Finishing the Sample

The wafer was then broken into pieces containing four structures each (four times four pads) and these pieces glued into chip carriers. The contacts on the chip carriers were connected to the corresponding pads on the sample with a bonder 4523AD. A backgate was added by scratching the SiO_2 layer of the wafer on an edge. The conducting Si showing under it was connected to the chip carrier by a drop of silver paint (Fig. 3.8). The whole Si layer of the wafer could now serve as a backgate creating an almost uniform field around the complete nanotube.

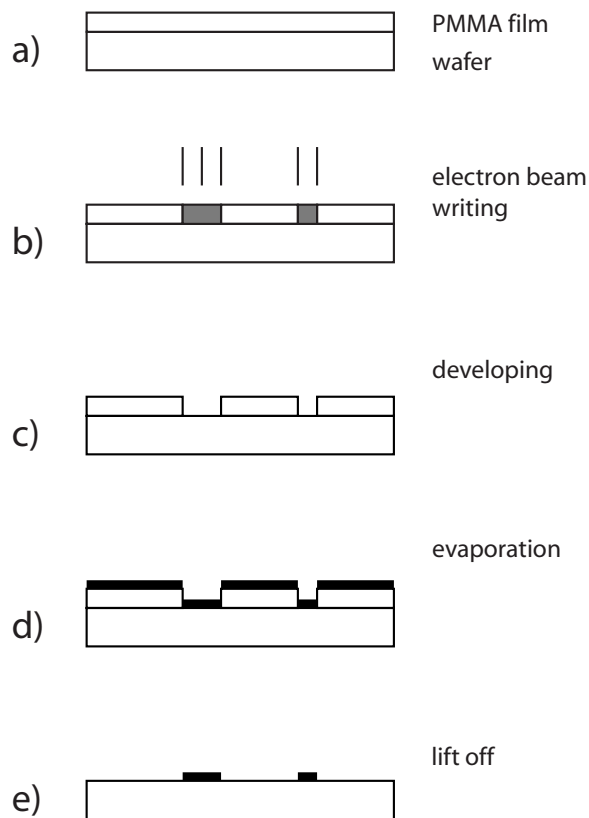


Figure 3.4: The five steps for the lithography lift-off process are: a) Application of a layer of PMMA to the wafer. b) Writing the structures into the PMMA. c) Developing the sample. PMMA previously exposed to the electron beam is dissolved. d) Application of the material for the structures by evaporating. e) Dissolving the remaining PMMA with acetone. All material on top of the PMMA is removed along with it.

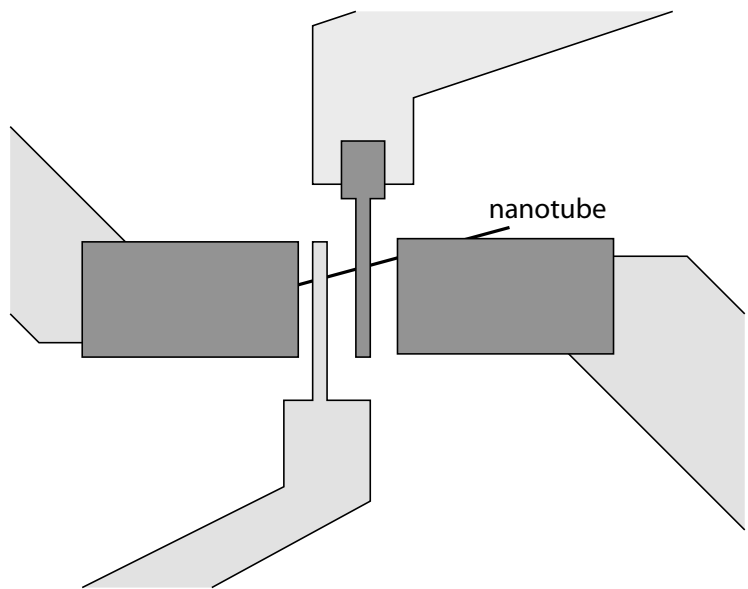


Figure 3.5: This sketch should help to clarify the lithography structure of the second sample: While the light grey areas have an isolating SiO₂ layer at the bottom, the dark grey areas consist only of Pd and thus establish contact.

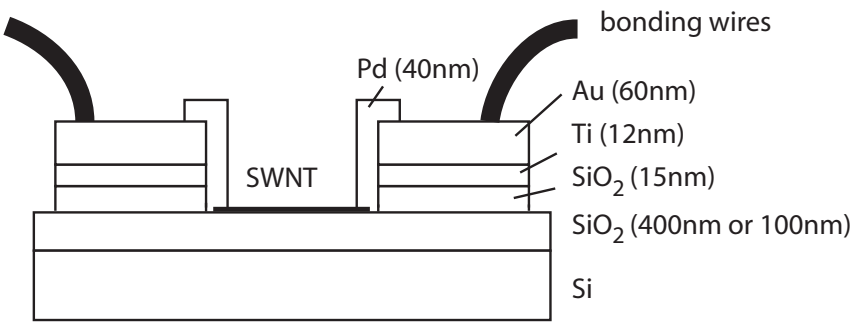


Figure 3.6: Bonding wires connect the pads with the chip and the rest of the experiment.

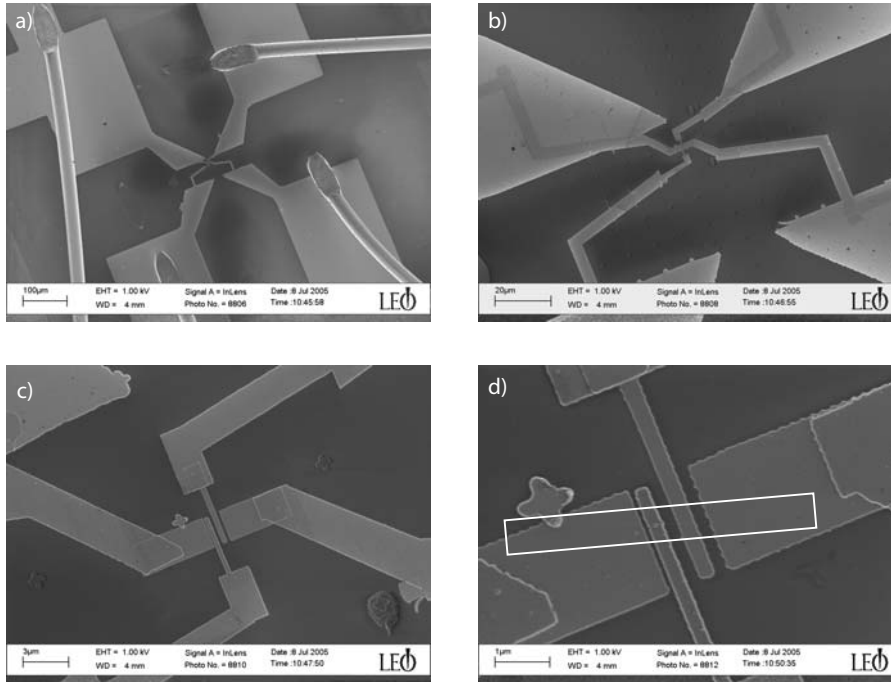


Figure 3.7: a) One pad quartet with one nanotube. Clearly visible are the bonding wires at the rim and the inner X-shaped structure. b) The X consists of four arms that do not touch. The upper left and the bottom right arms make contact with the tube, the other two are a topgate and a barrier that divides the nanotube in two halves. c) The inner structure was not done in one lithography step. While the arms of the X and the topgate (from the bottom) do not make electrical contact with the surface due to a layer of isolating SiO_2 , the smaller rectangles and the barrier (from the top) consist of Pd and connect the tube with the rest of the device. d) The tube itself is hardly recognizable. For better visibility a frame is drawn around it.

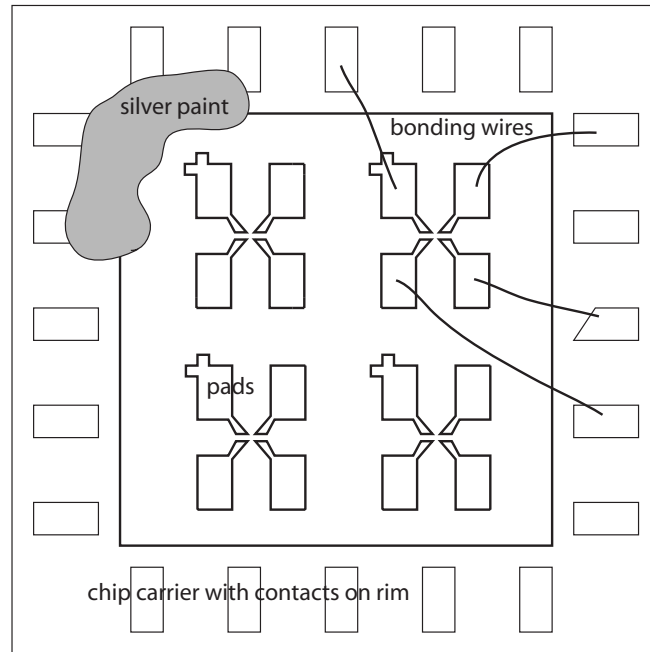


Figure 3.8: This sketch shows how the pads are connected to the chip contacts. The silver paint connects several contacts to the Si layer of the wafer since the SiO_2 is scratched there. The whole Si layer can therefore act as a backgate.

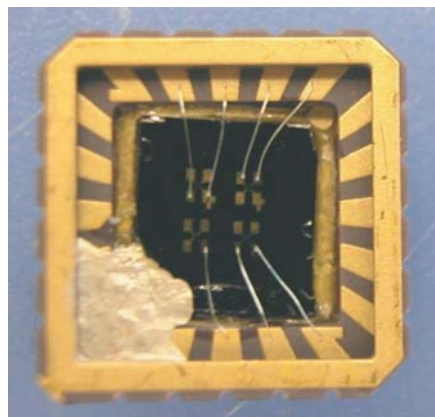


Figure 3.9: A photograph of a chip carrier showing the silver paint (bottom left) and bonding wires leading from the contacts on the rim of the chip carrier to the corresponding pads on the wafer.

Chapter 4

Experimental Setup and Measurements

4.1 Precautions During Experimental Setup

As soon as the sample is connected to the contacts on the chip carrier, great care is necessary not to destroy the nanotube with a casual touch (electrical shock). Every potential difference on the chip carrier would produce a current that has to flow through a bonding wire and over a pad to the tube, through it, and on its other side via another pad and its bonding wire back to the chip carrier. A potential difference of as little as 1 V can be enough to burn the nanotube.

Each manipulation has therefore to be carried out with a grounded instrument. Tweezers can be grounded by a clip and a wire, the operators themselves by wrist bands that contain a piece of metal which again is connected to the ground by a wire. All devices have a connection to the ground that gets switched off only directly before a measurement. In this way, as little current as possible flows through the nanotube.

4.2 Testing the Samples

Many samples have defects that do not show up under the microscope. The surface of the wafer may be scratched, the nanotube can have flaws or impurities that affect its conducting behavior, or the lithographic structures have not been placed precisely enough. In order to find out which samples really work, the chip carrier is first inserted into a sample test box (Fig. 4.1). In this device, little currents are measured at room temperatures to determine the resistance of the nanotubes.

The sample test box is grounded when the chip carrier is built in. The connections to the ground are switched off only just before a measurement. Each switch is controlling all lines on one side except for the four middle

ones which depend on the fifth switch in the middle of the box. Every line refers to one of the contacts on the chip carrier so one can select the required contacts depending on where the bonding wires end on the chip.

In a first step, the resistance of the nanotube is measured via source and drain. The theoretical maximum value is given by $4e^2/h = 6.5\text{ k}\Omega$, but anything under $100\text{ k}\Omega$ is considered very good. If the resistance is significantly higher than $100\text{ k}\Omega$, say $1\text{ M}\Omega$, the nanotube could still be a semiconducting device residing in the band gap. Applying a voltage to the backgate and changing the background potential can help decide whether this is the case. If the resistance does not decrease, it must be assumed that some component of the device is broken.

In case of good conductance, a second step must determine whether the current really flows through the nanotube or whether there is some connection of the device to the backgate. This may happen for instance when the surface of the wafer is scratched and the isolating layer of SiO_2 is damaged. For this measurement, one of the wires is now attached to the backgate. The resistance between source/drain and the backgate should be in the $\text{G}\Omega$ regime, but the setup just indicates whether it is much greater than the built-in dropping resistor ($R = 10\text{ M}\Omega$). If this is the case, the sample is assumed to be working. When there are more components to the device (as in my second sample), each connection is then tested individually to check for shortcuts.

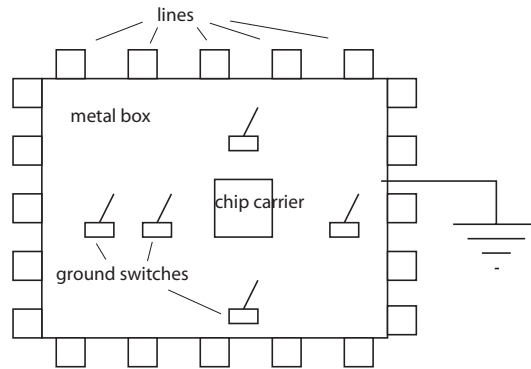


Figure 4.1: A sketch of the sample test box. The sample is inserted into the socket on top of the box. Around the box are the lines where wires from and to the lock in/receiver can be attached.

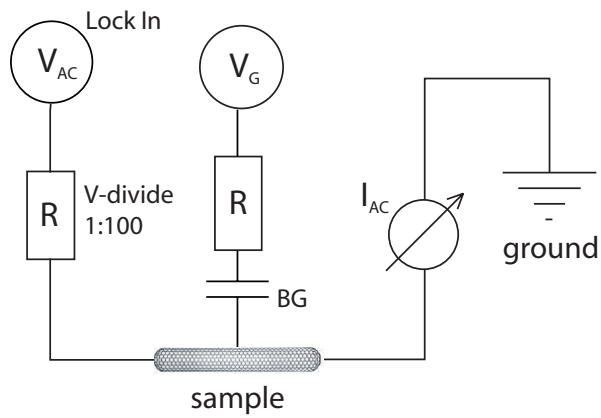


Figure 4.2: Schematic of the setup for sample testing. The drawing of the tube is taken from [3]

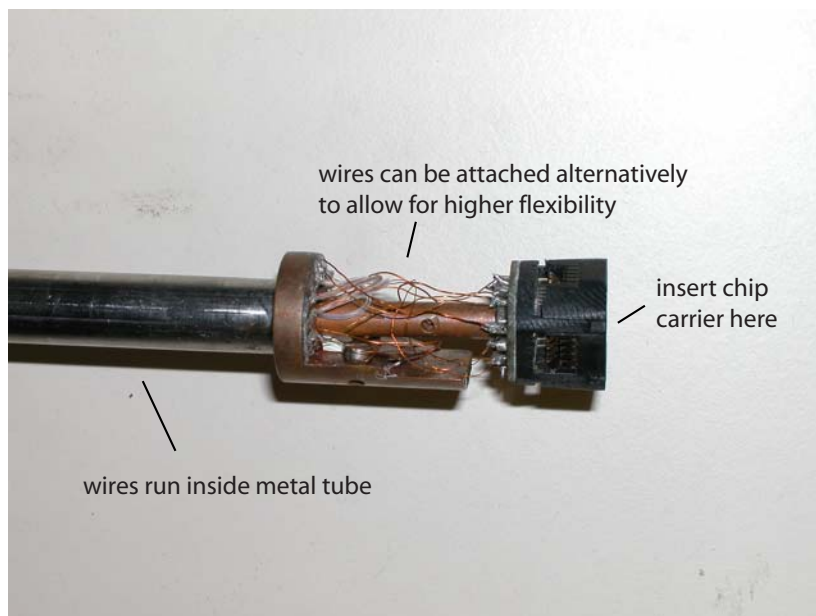


Figure 4.3: The end of the dipstick where the chip carrier is fastened.

4.3 Low-Temperature Measurements

One of the working samples is chosen for low-temperature conductance measurements. The sample is attached to the tip of a dipstick (Fig. 4.3) and put into a Dewar vessel (Cryofab CMSH-100) containing liquid ^4He . The evaporation temperature of ^4He is approximately 4.2 K, so the interior of the vessel is at that temperature as long as some of the Helium remains liquid. As explained in the theory chapter, this should make it possible to discern equally spaced peaks of tunneling conductance.

4.4 The First Sample

The first sample was finished by the end of April and had a SiO_2 -layer with a thickness of 400 nm. The lithographic structure was comparably simple, involving only one step beyond the pads and crosses. The nanotube was contacted by a source and a drain, while the Si layer of the wafer served as a backgate.

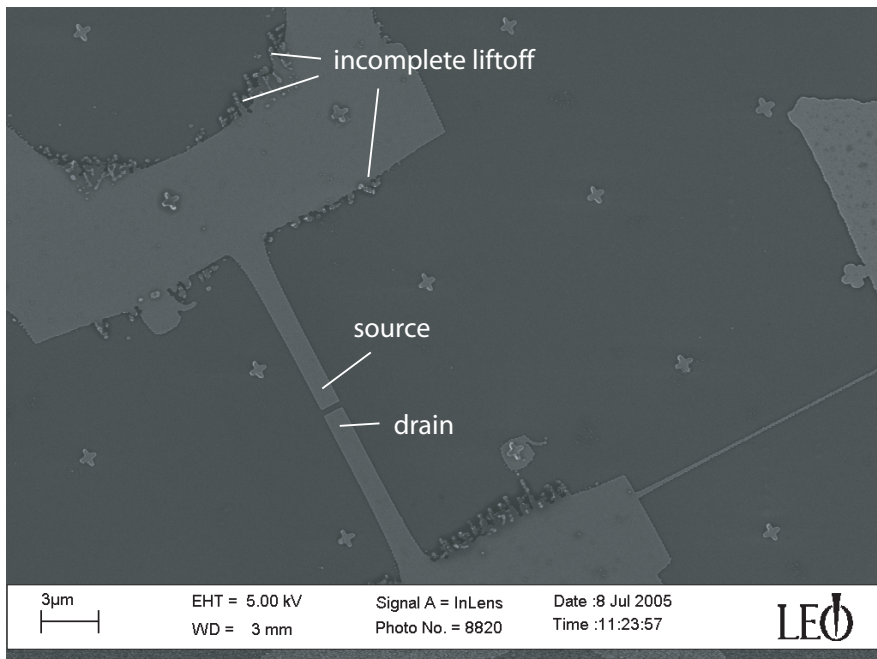


Figure 4.4: The lithographic structure of the first sample was quite simple with only two contacts serving as source and drain.

Of the 16 candidates on the wafer, only two were conducting at all. The chosen sample had a resistance of roughly $270\text{ k}\Omega$ and no contact to the backgate. Application of voltage to the backgate revealed that the nanotube

was semiconducting. On Fig. 4.5 two of the backgate voltage sweeps at 300 K (room temperature) are depicted.

a) shows a sweep between -20 V and 20 V with the band gap roughly between -5 V and 5 V. On the left of it is the valence band (p-region), right the conductance band (n-region). The nanotube shows very nicely the characteristics of a ambipolar field effect transistor. The visible oscillations are noise, Coulomb oscillations are not detectable at room temperature since thermal energies are too big compared to the charging energy or the level spacing.

b) depicts another measurement of the same sample. The backgate voltage ranges from -10 V to 20 V, but due to charging effects on the device (hysteresis), the band gap has shifted and starts in this case at a backgate voltage of 15 to 18 V. What we see is a smaller hysteresis in the p-region. This is probably caused by electron injections of the nanotube into the SiO_2 layer at large gate voltages [14]. The charges are trapped inside the oxide until the polarity is reversed. Naturally, the presence of these charges has an effect on the electric field around the nanotube. The backgate voltage in b) starts at 10 V (blue line), goes to -10 V, from there to 20 V (pink line) and returns to 10 V (red line). Apparently an electron injection took place at roughly 20 V, causing the red line to leave the band gap at a higher backgate voltage. The hysteresis between the red and the pink line is clearly visible below that point. This effect is observable more easily at large temperatures (300 K) since at lower temperatures fewer charges are injected into the wafer.

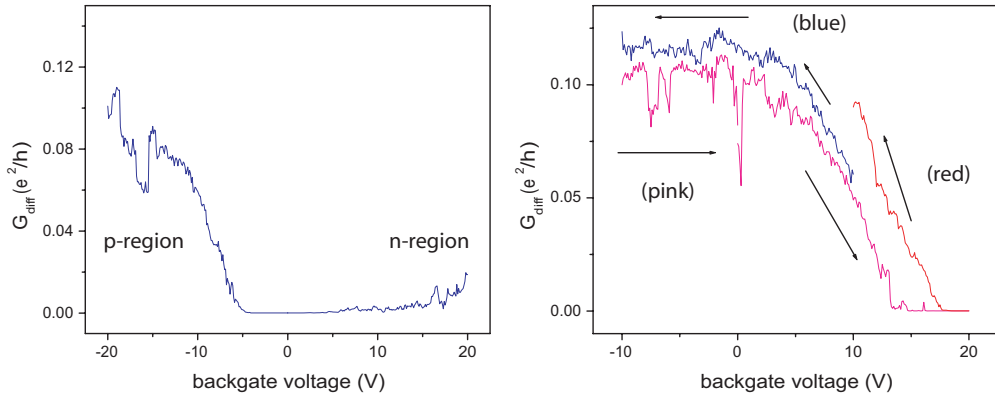


Figure 4.5: Two measurements at room temperature. a) The band gap between the p-region and the n-region. b) hysteresis in the p-region.

To my disappointment, the measurements at low temperatures showed

no Coulomb oscillations, only noise. It must be assumed that the contacts were not reliable under these low-temperature conditions.

4.5 The Second Sample

After measurements on the first sample were finished, a second experiment was started. This time the lithographic structure was more complex in order to create a double quantum dot system. The nanotube strip was divided into two parts by a center contact (source) between the two drain contacts (Fig. 4.7). Both parts could act as a quantum dot. Since individual control of the quantum dots was desired, a topgate was added to one of them that did not make contact, but was connected to the nanotube by a capacitance. The right dot could be manipulated by the backgate, while the field for the left dot was created by the backgate and the topgate together.

The reason why this setup is interesting is that when measuring the quantified discharging of a quantum dot, at some point the signal gets very weak due to low tunneling probability for particles deep within the potential well. With above setup it should be possible to discharge one dot while using the other as a detector. The two quantum dots are connected by a mutual capacitance C_m over the barrier. Because of this connection, they are sensitive for each others charge. With $Q = C \cdot U$ we get:

$$Q_1 = C_{g,1} \cdot V_{g,1} + \frac{C_m}{C_m + C_{g,2}} \cdot Q_2$$

So while using the detector dot in normally charged mode (with a good signal) we could still observe the complete discharging of the other dot from that signal.

Unfortunately, the wafer that had been used for these samples (with a SiO₂ layer thickness of 100 nm) suffered from a leakage problem to the backgate. Almost all devices had contact with the backgate which of course makes measurements impossible (or rather renders them meaningless). Contact of source/drain with the backgate is most commonly established when using the bonding machine to attach the bonding wires to the gold structure. It should be checked if changing the bonding parameters can help avoid this problem.

As a result of our devices having contact with the backgate, it was not possible to determine if our setup can act as a double quantum dot. Hopefully this will be done soon with better success.

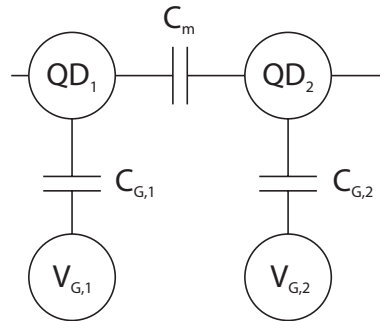


Figure 4.6: A double quantum dot. The dots are connected by a mutual capacitance C_m .

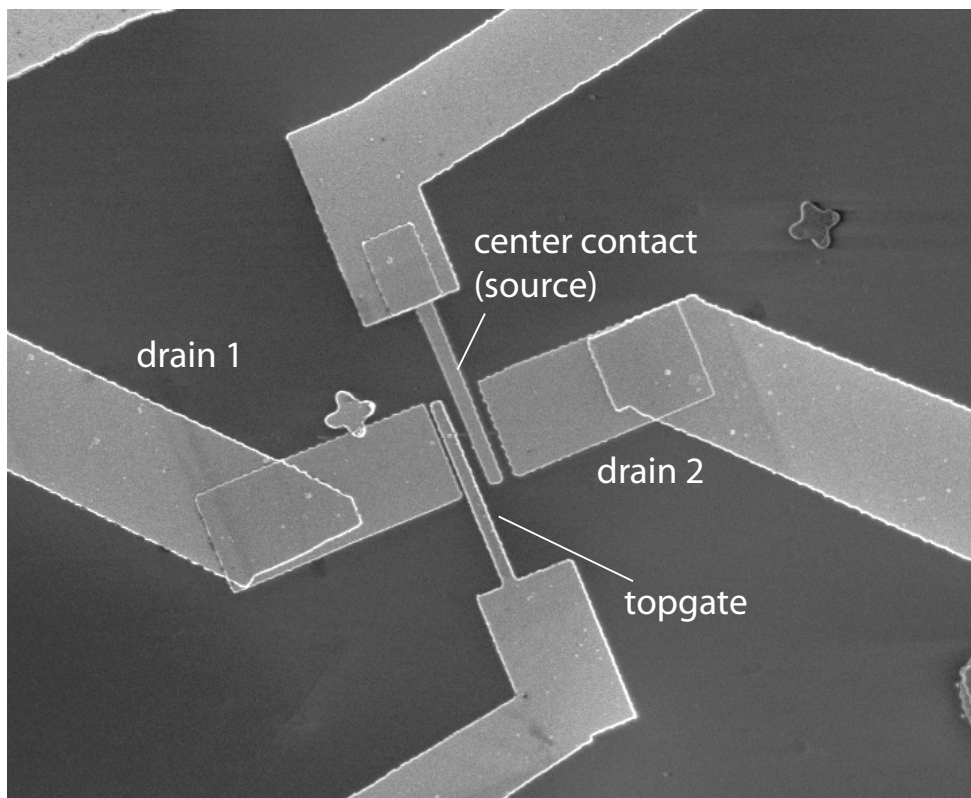


Figure 4.7: On this photo the source, drain, topgate, and barrier contacts are clearly visible. The nanotube itself is a horizontal white line from source to drain.

Chapter 5

Summary and Thanks

5.1 Summary and Outlook

During my semester work I was mainly occupied with learning the techniques for growing, localizing, contacting and measuring nanotubes. Si-wafers with a layer of SiO₂ on top were broken into pieces and cleaned with various methods to gain a clean surface. The wafer was then inserted into an oven chamber that was flooded with methane gas at a temperature of 1000° C. Carbon atoms from the gas were absorbed by the surface and grew into nanotubes with lengths of up to several μm (Chemical Vapor Deposition). Successful growth was verified in a scanning electron microscope (LEO) before starting with application of metallic structures.

Using electron beam lithography, metallic structures were applied to the surface in several steps in order to gain a conducting structure with a nanotube at the center. This structure contained a source and a drain contact and in some cases a topgate for more detailed control of the measurement.

The finished wafer was glued into a chip carrier and the structures on the surface connected to the chip carrier contacts via bonding wires. By adding some conducting silver paint to connect the Si layer of the wafer to some spare contacts on the chip carrier, a backgate was created.

The samples were tested for conductivity and contact to the backgate in a sample tester. For the best samples, measurements of the conductivity depending on the backgate voltage were made at different temperatures. One sample demonstrated very good ambipolar characteristics (FET) and hysteresis at room temperature but did not work under low temperatures due to bad contacts.

Judging from my experience I suggest that for the wafers with only 100 nm of SiO₂ on top the bonder parameters must be adjusted to avoid piercing the entire SiO₂-layer. The danger of a such an incident which establishes contact between source/drain and the backgate is much greater than for the wafers with 400 nm of SiO₂. Of the 5 samples with a 400 nm

SiO₂ layer that were tested, none had contact with the backgate, but of the 7 samples with 100nm 5 did have contact. Sadly, these were the late samples that were expected to act as double quantum dots. I believe that independently from our problem, the devices that we fabricated to measure double quantum dots could work well. The complex lithography structures were achieved with minimal problems and appear to be flawless.

A system similar to ours can possibly be realised using a 2DEG in a GaAs heterostructure. The nanotube quantum dot would there be part of a quantum point contact, influencing the conductivity of the 2DEG. I am looking forward to learning more about that system while working in that field during my masterwork.

5.2 Acknowledgements and Thanks

This completely new field of practical work presented me with challenges as well as numerous moments of motivation. Parallel to my own project, I could watch other experiments and was given generous information and advice by the members of the team. I want to thank all of them, especially of course my mentor Matthias Gräber who was a good teacher and a patient guide for my project. I am also very grateful to Professor Schönenberger for providing the opportunity to work in such an interesting and topical field.



Figure 5.1: Thanks to all, also those who are not on this photo.

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Appendix A

Numbers and Descriptions

A.1 Wafer

Wafer Material

Resistivity (Ωcm): 0.003-0.005

Type, Dopant: p, Boron

Back surface: Alkaline etched

Thickness (nm): 500-550

Thickness of SiO₂-layer (nm): 396±1 (first sample); 100±1 (second sample)

Ultrasonic Cleaner

Process: 10 minutes in 2-propanol in ultrasonic cleaner

UVO-Cleaner

Model: Model 42 by Jelight Company Inc.

Process: 10 minutes into UVO-cleaner on glass slides

Plasmalab

Model: Oxygen PLasmalab^{80Plus} by Oxford

Recipe: Recipe Number 5

Steps: Step 4 for 20 seconds, 100 W, $5 \cdot 10^{-5}$ bar; step 20 (venting chamber)

A.2 Nanotube Growth

Catalyst

Composition: Al₂O₃ (0.0375 mg/ml); Fe(NO₃)₃·9H₂O (0.1163 mg/ml); MoCl₂O₂ (0.0338 mg/ml)

Process: Shake catalyst during 2 hours on magnetic stirrer; leave standing for 10 minutes; apply process number 2 (spinner)

Chemical Vapor Deposition (CVD)

Oven Temperature: 1000° C

Argon flow: 1041/h

Growth period (methane flow): 10 minutes

A.3 Lithography

PMMA

Composition: Chlorobenzene (60%), Polymethylmethacrylat (40 %)

Thickness of layer: 600 nm

Process for application: Stir mixture for 10 minutes; process number 2 (spinner); bake in oven (180° C) for at least 45 minutes

JEOL

Model: JSM-IC848

PROXY WRITER Parameters for first sample: alex.par

Structure for first sample: normalalex1.gdb (crosses); normalalex2.gdb (pads); cvdv.gdb; cvdh.gdb

PROXY WRITER Parameters for second sample: matt.par

Structure for second sample: normalalex1.gdb (crosses); normalalex2.gdb (pads); alex1tgv.gdb + tg1vcont.gdb; alex1tgh.gdb + tg1hcont.gdb

Magnification for writing: Magnification 500 for crosses; magn. 25 for pads; magn. 250 for contacts

Current adjustment: 53 pA at magnification 300'000 on FaradCup

Compensation parameters: Anglex = 7.8; angley = 8.1

Developing

Process: Dip sample into E-Beam resistant (75 seconds); then into 2-propanol (75 seconds)

Evaporation

Model: PLS 500 evaporator by Balzers-Pfeiffer

Parameters:

Material	P_B (mbar)	P_E (mbar)	Rate ($\text{\AA}/\text{s}$)	I_{Gun} (mA)	d (\AA)
SiO ₂	$4 \cdot 10^{-7}$	$9 \cdot 10^{-7}$	3.4	12	150
Ti	$3.4 \cdot 10^{-7}$	$2 \cdot 10^{-7}$	1.8	59	120
Au	$2.6 \cdot 10^{-7}$	$5 \cdot 10^{-7}$	2.5	309	600
Pd	$8.5 \cdot 10^{-8}$	$2.5 \cdot 10^{-7}$	2.1	44	400

A.4 Bonder

Parameters

Model: 4523AD by CMTec

Search: 3.05

Power: 1.76

Time: 4.5

Force: 1.2

Step: 2.9

Kink: 0.0

Reverse: 0.0

Yspeed: 1.0

Loop: 3.0

A.5 Dewar

Model: CMSH-100 by Cryofab